# SIS3820-CLOCK
# VME Clock Distributor
# Version E205

# User Manual

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# Revision Table:

| Revision | Date | Modification |
|---|---|---|
| 1.00 | 01.08.2008 | Derived from SIS3820 Clock version 0x3820e003 manual |
| 1.01 | 31.03.2010 | 0x E204 firmware, new mode 32 start/stop outputs |
| 1.10 | 21.12.2010 | 0x E205 firmware, add programmable delay in sync. mode |
| 1.11 | 16.03.2011 | Add missing descriptions to status register bits |

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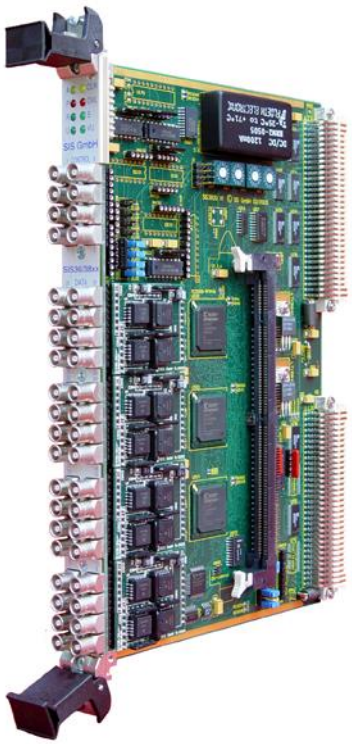
## 2 Introduction

The SIS3820-CLOCK board firmware was developed to distribute clock and start/stop signals to up to 32 SIS330x digitizer boards.



# 3 Technical Properties/Features

This manual describes the implemented functionality for the SIS3820-CLOCK firmware. Other firmware designs are SIS3820 (multi purpose scaler) and SIS3820-LATCH (input register with counter and interrupt functionality)

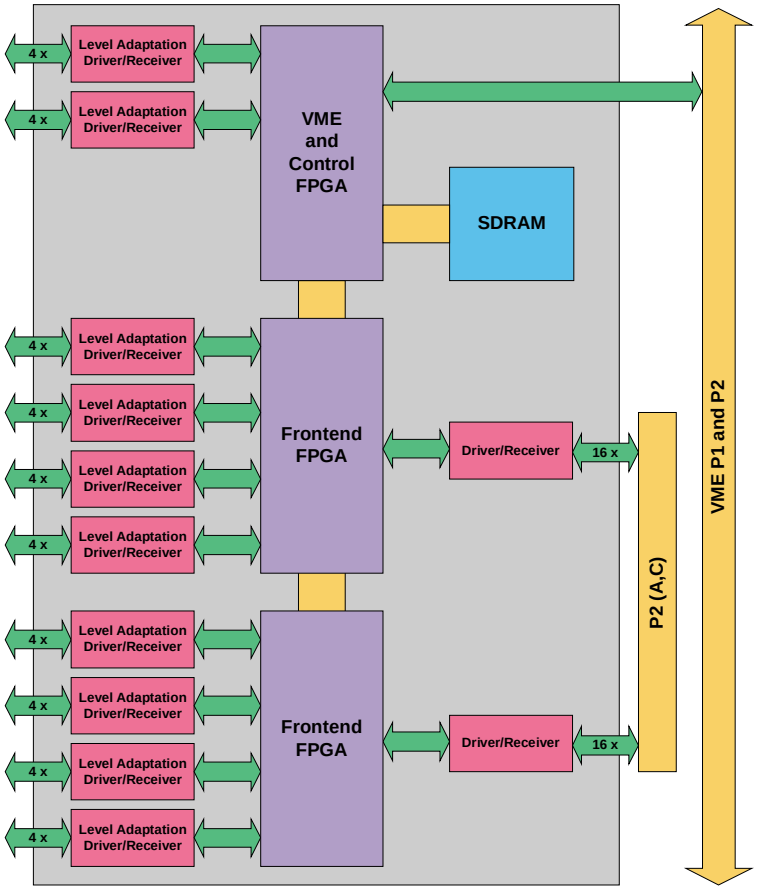
Find below a list of key features of the SIS3820-CLOCK.

- 32 channel clock output or
- 16 channel clock and 16 channel start/stop/gate output or
- 32 channel start/stop output
- NIM LEMO outputs (others on request)
- P2 output option
- A16/A24/A32/D32
- Geographical addressing mode (in conjunction with VME64x backplane)
- Hot swap (in conjunction with VME64x backplane)
- VME64x Connectors
- VME64x Side Shielding
- VME64x Front panel
- VME64x extractor handles (on request)
- single supply (+5 V)
- in field firmware upgrade capability

# 4 Functionality

The functionality of the SIS3820 is a combination of hardware (printed circuit board) design, stuffing options and firmware. The module consists of two FPGAs that hold the frontend logic and on FPGA that holds the VME interface, the SDRAM controller and the control logic functions. Logic level adaptation is handled by classic DIL components and single inline (SIL) resistor networks. The firmware is loaded from a serial PROM at power up. Both JTAG and VME can be used for in field firmware upgrades/changes.

## *4.1 Block Diagram*



# 5 Getting started

This section is intended for the first time SIS3820-CLOCK user..

## 5.1 Installation

- Select addressing mode with J1 (factory default is A32)
- Select base address with SW1 through SW4 in non geographical addressing (the default base address setting is 0x38000000)
- turn VME crate power off
- install your SIS3820-CLOCK board in the VME crate
- connect inputs and outputs
- turn VME crate power back on
- verify, that the P (power) and R (ready) LEDs are on and all other LEDs are off after the approximately 2s long power up self test cycle

## *5.2 Initial VME access test*

Both the user LED and readout of the Module Id. and firmware register provide a good way to verify that proper initial communication with the SIS3820 can be established.

## *5.3 Setup example*

A typical setup consists of the VME write accesses listed below.

| VME address | Datum |
|---|---|
| base+0x60 | arbitrary |
| base+0x10 | 0x180 |
| base+0x14 | 0x8082 |
| base | 0x8083 |

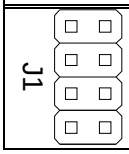
It activates the following functions

- strobe length 1 (2 clock ticks)
- Front panel outputs
- General enable
- 16 clock/16 start/stop gate outputs
- 100 MHz internal clock
- user LED on
- strobe signal on control 2 input

This setup sequence can be found for the SIS1100/3100 PCI to VME interface in the file sis3820clock_setup.c on the SIS36/38xx CDROM

# 6 VME Addressing

The SIS3820 firmware addressing concept is a pragmatic approach to combine standard rotary switch style settings with the use of VME64x backplane geographical addressing functionality.
The base address is defined by the selected addressing mode, which is defined by jumper array J1 and possibly SW4 and SW1 (in non geographical mode).

| | Function |
|---|---|
|   | EN_A32 |
| | EN_A24 |
| | EN_GEO |
| | EN_A16 |

| EN_A32 | EN_A24 | EN_GEO | EN_A16 | Description |
|---|---|---|---|---|
| X | 0 | 0 | 0 | A32 addressing, address compared withSW4–SW 1 |
| X | 0 | x | 0 | A32 addressing, address compared with geographical address |
| 0 | x | 0 | 0 | A24 addressing, address compared withSW2/SW1 |
| 0 | 0 | 0 | x | A16 addressing, address compared withSW2/SW1 |
| 0: jumper open, x: jumper closed | | | | |

The tables below illustrates the possible base address settings.

| EN A32 | EN A24 | EN GEO | EN A16 | Bits | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| x | 0 | 0 | 0 | SW4 | | | | SW3 | | | | SW2 | | | | SW1 | | | |
| x | 0 | x | 0 | 0 | 0 | 0 | GA4 | GA3 | GA2 | GA1 | GA0 | 0 | | | | 0 | | | |
| 0 | x | 0 | 0 | y | | | | y | | | | SW2 | | | | SW1 | | | |
| | | | | Bits | | | | | | | | | | | | | | | |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | x | SW2 | | | | SW1 | | | | A | | | | A | | | |

| Shorthand | Explanation |
|---|---|
| SW1-SW4 | Setting of rotary switch SW1 to SW4 |
| Y | don't care |
| GA0-GA4 | Geographical address bit as defined by the VME64x(P) backplane |
| A | Modules address space |

**Notes:**

- This concept allows the use of the SIS3820 in standard VME as well as in VME64x environments, i.e. the user does not have to use a VME64x backplane.
- The factory default setting is 0x38000000 (i.e. SW4=3, SW3=8, EN_A32 closed, EN_GEO, EN_A24 and EN_A16 open/disabled)

### 6.1 Address map

| Offset | R/W | Mode | Function/Register |
|---|---|---|---|
| 0x0 | R/W | | Control/Status register |
| 0x4 | R/W | | Module Id. and firmware revision register |
| reserved | R/W | | One wire Id. register |
| 0x10 | R/W | | Clock source registers |
| 0x14 | R/W | | Clock frequency register |
| 0x18 | R/W | | Delay register |
| | | | |
| 0x60 | W | | Key Reset (General Reset) |
| 0x64 | W | | Key Clock (Issue single 20 ns clock pulse) |
| 0x68 | W | | Key Strobe (Issue single start/stop/gate pulse) |
| 0x6C | W | | Key DLL Reset |
| | | | |
| 0x310 | R/W | | XILINX JTAG_TEST/JTAG_DATA_IN |
| 0x314 | W | | XILINX JTAG_CONTROL |

The shorthand KA stands for key address. Write access with arbitrary data to a key address initiates the specified function

# 7 Register description

The function of the individual registers is described in detail in this section.

## *7.1 Control/Status Register(0x0, write/read)*

The control register is in charge of the control of several basic properties of the SIS3820-CLOCK board. It is implemented via a selective J/K register, a specific function is enabled by writing a 1 into the set/enable bit, the function is disabled by writing a 1 into the clear/disable bit (which location is 16-bit higher in the register). An undefined toggle status will result from setting both the enable and disable bits for a specific function at the same time.
On read access the same register represents the status register.

| Bit | write Function | read Function |
|---|---|---|
| 31 | General Disable Logic (*) | 0 |
| 30 | clear reserved 14 (*) | 0 |
| 29 | clear reserved 13 (*) | 0 |
| 28 | clear reserved 12 (*) | 0 |
| 27 | clear reserved 11 (*) | 0 |
| 26 | clear Frontpanel start/stop mode (*) | 0 |
| 25 | disable input inversion (*) | 0 |
| 24 | disable external Strobe Veto (*) | 0 |
| 23 | disable front panel outputs (*) | 0 |
| 22 | disable P2 output (*) | 0 |
| 21 | clear P2 Strobe Mode Bit | 0 |
| 20 | clear Double Output Clock Mode (*) | 0 |
| 19 | clear Control Output 8 (*) | 0 |
| 18 | clear Control Output 7 (*) | 0 |
| 17 | select Frontpanel clock mode (*) | 0 |
| 16 | switch off user LED (*) | 0 |
| 15 | General Enable Logic | Status General Enable Logic<br>0=off, 1=on |
| 14 | set reserved 14 | Status reserved 14 |
| 13 | set reserved 13 | Status reserved 13 |
| 12 | set reserved 12 | Status reserved 12 |
| 11 | set reserved 11 | Status reserved 11 |
| 10 | select Frontpanel start/stop mode on odd channels | Status start/stop mode on odd channels<br>0=clock, 1=start/stop |
| 9 | set input inversion | Status input inversion |
| 8 | set external Strobe Veto | Status external Strobe Veto |
| 7 | enable front panel outputs | Status front panel output enable |
| 6 | enable P2 outputs | Status P2 output enable |
| 5 | set P2 Strobe Mode Bit | Status P2 Strobe Mode Bit |
| 4 | set Double Output Clock Mode | Status Double Output Clock Mode |
| 3 | set Control Output 8 | Status Control Output 8 |
| 2 | set Control Output 7 | Status Control Output 7 |
| 1 | select Frontpanel start/stop mode on even channels | Status start/stop mode on even channels<br>0=clock, 1=start/stop |
| 0 | switch on user LED | Status User LED (1=LED on, 0=LED off) |

(*) denotes power up default setting, i.e. the power up reading of the register is 0x0

external Strobe Veto: 0: no Veto for Control Input 2 and 3
1: Control Input 2 and 3 vetoed/disabled

P2 Strobe Mode Bit: 0: "Strobe signal"** routed to P2 START
Control Input 3 routed to P2 STOP
1: "Strobe signal"** routed to P2 STOP
Control Input 3 routed to P2 START

** origin of "Strobe signal" depends on "Strobe Source Bits" and " Strobe Mode Bits"

P2 outputs : 0: P2 output signals are disabled
1: P2 output signals are enabled

Front panel outputs: 0: front panel output signals are disabled
1: front panel output signals are enabled

Front panel clock and start/stop table:

| Setting of Bit 10 start/stop | Setting of Bit 1 clock and start/stop | Signal on even channels 2,…, 32 | Signal on odd channels 1,…,31 |
|---|---|---|---|
| 0 | 0 | clock | clock |
| 0 | 1 | start/stop | clock |
| 1 | 0 | clock | start/stop |
| 1 | 1 | start/stop | start/stop |

Set Double Output Clock Mode : 0: normal output clock
1: double output clock (DLL, delay locked loop)

**Note: A DLL reset has to be issued after a change of the clock source in double frequency output mode**

**Valid source clock range: 25 to 100 MHz**

## *7.2 Module Id. and Firmware Revision Register (0x4, read)*

This register reflects the module identification of the SIS3820 and its minor and major firmware revision levels. The major revision level will be used to distinguish between substantial design differences and experiment specific designs, while the minor revision level will be used to mark user specific adaptations.

| Bit | Function | Reading |
|---|---|---|
| 31 | Module Id. Bit 15 | 3 |
| 30 | Module Id. Bit 14 | |
| 29 | Module Id. Bit 13 | |
| 28 | Module Id. Bit 12 | |
| 27 | Module Id. Bit 11 | 8 |
| 26 | Module Id. Bit 10 | |
| 25 | Module Id. Bit 9 | |
| 24 | Module Id. Bit 8 | |
| 23 | Module Id. Bit 7 | 2 |
| 22 | Module Id. Bit 6 | |
| 21 | Module Id. Bit 5 | |
| 20 | Module Id. Bit 4 | |
| 19 | Module Id. Bit 3 | 0 |
| 18 | Module Id. Bit 2 | |
| 17 | Module Id. Bit 1 | |
| 16 | Module Id. Bit 0 | |
| 15 | Major Revision Bit 7 | |
| 14 | Major Revision Bit 6 | |
| 13 | Major Revision Bit 5 | |
| 12 | Major Revision Bit 4 | |
| 11 | Major Revision Bit 3 | |
| 10 | Major Revision Bit 2 | |
| 9 | Major Revision Bit 1 | |
| 8 | Major Revision Bit 0 | |
| 7 | Minor Revision Bit 7 | |
| 6 | Minor Revision Bit 6 | |
| 5 | Minor Revision Bit 5 | |
| 4 | Minor Revision Bit 4 | |
| 3 | Minor Revision Bit 3 | |
| 2 | Minor Revision Bit 2 | |
| 1 | Minor Revision Bit 1 | |
| 0 | Minor Revision Bit 0 | |

### 7.2.1 Major revision numbers

Find below a table with major revision numbers used to date

| Major revision number | Application/user |
|---|---|
| 0x01 | Generic SIS3820 32 channel scaler design |
| 0xE0 | SIS3820-CLOCK (U580 : 40 MHz osc. ) |
| 0xE2 | SIS3820-CLOCK (U580 : 100 MHz osc. ) |
| 0xF0 | SIS3820-LATCH |

### *7.3 Clock Source Register(0x10, write/read)*

This register is used to chose among the three clock sources and to define the clock multiply/divide factor or the use of the clock frequency register..

| Bit | write Function | read Function |
|---|---|---|
| 31 | reserved | 0 |
| 30 | reserved | 0 |
| 29 | reserved | 0 |
| 28 | reserved | 0 |
| 27 | reserved | 0 |
| 26 | reserved | 0 |
| 25 | reserved | 0 |
| 24 | reserved | 0 |
| 23 | reserved | 0 |
| 22 | reserved | 0 |
| 21 | reserved | 0 |
| 20 | reserved | 0 |
| 19 | reserved | 0 |
| 18 | reserved | 0 |
| 17 | reserved | 0 |
| 16 | reserved | 0 |
| 15 | Strobe Output Length Bit 7 | Status Strobe Output Length Bit 7 |
| 14 | .. | .. |
| 13 | .. | .. |
| 12 | .. | .. |
| 11 | .. | .. |
| 10 | .. | .. |
| 9 | .. | .. |
| 8 | Strobe Output Length Bit 0 | Status Strobe Output Length Bit 0 |
| 7 | Strobe Mode Bit | Status Strobe Mode Bit |
| 6 | Strobe Source Bit | Status Strobe Source Bit |
| 5 | Clock Divider Mode Bit 1 | Status Clock Divider Mode Bit 1 |
| 4 | Clock Divider Mode Bit 0 | Status Clock Divider Mode Bit 0 |
| 3 | Reserved | 0 |
| 2 | Reserved | 0 |
| 1 | Clock Source Bit 1 | Status Clock Source Bit 1 |
| 0 | Clock Source Bit 0 | Status Clock Source Bit 0 |

the power up default setting is 0x0

**Note:** the user has to keep in mind, that not all clock speeds may be supported by a particular digitizer

## Strobe Mode Bit

| Strobe Mode Bit | Clock Divider Mode |
|---|---|
| 0 | Direct Strobe:<br>Strobe signal (External Input or VME Key Strobe) is routed to the outputs directly (with a typical delay of 25 ns) |
| 1 | Programmed Strobe:<br>The leading edge of the Strobe signal generates a Strobe Output signal.<br>This Strobe Output signal is synchronized with the used clock. The length of the Output pulse is programmable from 1 to 256 clocks (Strobe Output Length Bits)<br>**Note:** its recommended to use a minimum setting of 1 (i.e. an output length of 2 clocks) with the SIS330x digitizers |

## Strobe Source Bits

| Strobe Source Bit | Clock Divider Mode |
|---|---|
| 0 | Use External Strobe Input (Control Input 2) |
| 1 | Use VME Key Strobe |

## Clock Divider Modes

| Clock Divider Mode Bit 1 | Clock Divider Mode Bit 0 | Clock Divider Mode |
|---|---|---|
| 0 | 0 | Straight clock |
| 0 | 1 | ½ clock |
| 1 | 0 | ¼ clock |
| 1 | 1 | Use clock frequency register |

## Clock Sources

| Clock Source Bit 1 | Clock Source Bit 0 | Clock Source |
|---|---|---|
| 0 | 0 | Internal 100 MHz (generated with DLL) |
| 0 | 1 | Second internal 100 MHz (U580) |
| 1 | 0 | External Clock Input |
| 1 | 1 | VME Key Clock |

Note:
The internal 100 MHz is generated with a DLL in the FPGA from the internal 50 MHz.
To get a better resolution use the “Second internal 100 MHz” instead of “internal 100 MHz”.
(U580 must be assembled with a 100 MHz 3.3 V oscillator)

### *7.4 Clock Frequency Register(0x14, write/read)*

This register is used to program the output frequency in “double ticks” of the selected clock. In conjunction with the SIS330x digitizer it will be used in combination with random clock mode in most cases to sample at clock speeds below the specified minimum Analog to Digital converter clock.

| Bit | Function |
|---|---|
| 31 | reserved, read back as 0 |
| 30 | reserved, read back as 0 |
| 29 | reserved, read back as 0 |
| 28 | reserved, read back as 0 |
| 27 | reserved, read back as 0 |
| 26 | reserved, read back as 0 |
| 25 | reserved, read back as 0 |
| 24 | reserved, read back as 0 |
| 23 | Bit 23 of preset value |
| ... | ... |
| 0 | Bit 0 of preset value |

the power up default setting is 0x0

**Note:** the user has to keep in mind, that not all clock speeds may be supported by a particular digitizer

Output frequency = (frequency of clock source / ((N+1)x2))

**Example:**

Clock Sources = 00 // internal 100 MHz
Clock Divider Modes = 11 // use clock frequency register

Clock Frequency register = 0x4 will result an output clock of 10 MHz (100 MHz / ((4 + 1) x 2 ))

### *7.5 Start/Stop Delay Register(0x18, write/read)*

This register is used to delay the output signal in programmed strobe mode (i.e. strobe mode bit=1 set in the clock source register). No delay will be used with the register at the power up default value of 0. The start/stop signal will be delayed by N+1 with the register value set to N..

| Bit | Function |
|---|---|
| 31 | reserved, read back as 0 |
| 30 | reserved, read back as 0 |
| 29 | reserved, read back as 0 |
| 28 | reserved, read back as 0 |
| 27 | reserved, read back as 0 |
| 26 | reserved, read back as 0 |
| 25 | reserved, read back as 0 |
| 24 | reserved, read back as 0 |
| 23 | Bit 23 of delay value |
| ... | ... |
| 0 | Bit 0 of delay value |

the power up default setting is 0x0

**Note:** the user has to keep in mind, that not all clock speeds may be supported by a particular digitizer

### 7.6 JTAG_TEST register

```
#define SIS3820_JTAG_TEST    0x310                    /* write; D32;  */
```

This register is used in the firmware upgrade process over VME only. A TCK is generated upon a write cycle to the register.

| Bit | write Function |
|---|---|
| 31 | none |
| ... | ... |
| 4 | none |
| 3 | none |
| 2 | none |
| 1 | TMS |
| 0 | TDI |

### 7.7 JTAG_DATA_IN register

```
#define SIS3820_JTAG_DATA_IN    0x310                  /* read; D32;  */
```

This register is used in the firmware upgrade process over VME only. It is at the same address as the JTAG_TEST register and is used in read access. It operates as a shift register for TDO. The contents of the register is shifted to the right by one bit with every positive edge of TCK and the status of TDO is transferred to Bit 30. Bit 31 reflects the current value of TDO during a read access.

### 7.8 JTAG_CONTROL register

```
#define SIS3820_JTAG_CONTROL    0x314                   /* write only; D32;
*/
```

This register is used in the firmware upgrade process over VME only.

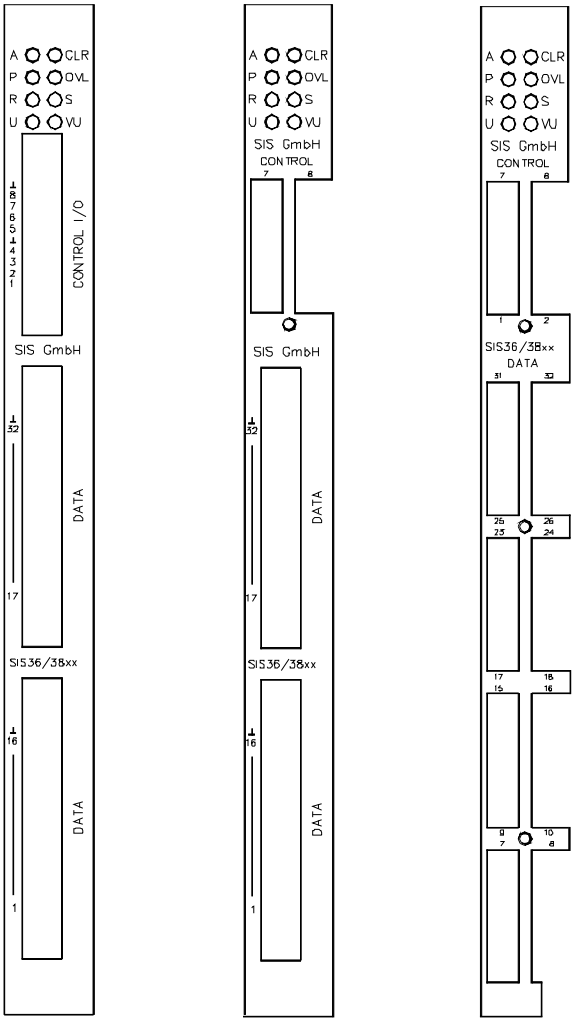
| Bit | write Function |
|---|---|
| 31 | none |
| ... | ... |
| 4 | none |
| 3 | none |
| 2 | none |
| 1 | none |
| 0 | 1: Enable JTAG output |

# 8 Front panel elements

## *8.1 Front Panel Layout*

The front panel of the SIS3820 is equipped with 8 LEDs, 8 control in- and outputs and 32 frontend in/outputs. On flat cable units (ECL and TTL) the control connector is a 20 pin header flat cable connector and the channel inputs are fed via two 34-pin headers. On LEMO (NIM and TTL) units the control in- and outputs are grouped to one 8 channel block and the counter inputs are grouped into 2 blocks of 16 channels. A mixed LEMO control/flat cable counter input version is available also. The units are 4 TE (one VME slot) wide, the front panel is of EMC shielding type. VIPA extractor handles are available on request or can be retrofitted by the user, if he wants to change to a VIPA crate at a later point in time.
In the drawing below you can find the flat cable (left hand side), the LEMO control/flat cable input (middle) and LEMO front panel layouts.

**Note: Only the aluminium portion without the extractor handle mounting fixtures is shown**

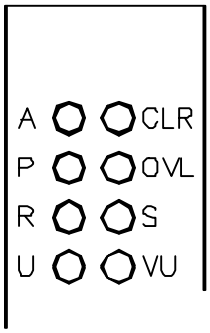


## 8.2 Front Panel LEDs

The SIS3820 has 8 front panel LEDs to visualize part of the units status. Three LEDs according to the VME64xP standard (Power, Access and Ready) plus 5 additional LEDs.

| Designation | LED | Color | Function |
|---|---|---|---|
| A | Access | yellow | Signals VME access to the unit |
| P | Power | red | Flags presence of VME power |
| R | Ready | green | Signals configured logic |
| U | VME user LED | green | To be switched on/off under user program control |
| CLR | Clock | yellow | Clock |
| OVL | | red | Strobe (Start/Stop/Gate) |
| S | Start/Stop | green | Enable P2 Output |
| VU | VIPA user LED | green | Front panel Output Enable |

The LED locations are shown in the portion of the front panel drawing below.




The VME Access, Clock and Start/Stop/Gate LEDs are monostable (i.e. the duration of the on phase is stretched for better visibility), the other LEDs reflect the current status.
A LED test cycle is performed upon power up (all LEDs except Ready LED on for some 2 s).

## 8.3 Control Inputs

The control input/output section has up to 4 inputs and up to 4 outputs.

| Control Signal | Function | Comment |
|---|---|---|
| 1 | external clock input | |
| 2 | start/stop/gate | front panel and P2 start |
| 3 | stop | P2 stop only |
| 4 | not used | |
| 5 | not used | |
| 6 | not used | |
| 7 | output 7 | set/clear via control register |
| 8 | output 8 | set/clear via control register |

## *8.4 Front panel Outputs*

The SIS3820-CLOCK supports 2 output modes, which are selected with bit 1 of the control register.

- 32 x clock outputs (power up default)
- or 16 x clock and 16 x start/stop/gate outputs

### 8.4.1 32 clock output mode

The selected clock source is fanned out to all 32 front panel outputs in this mode of operation.

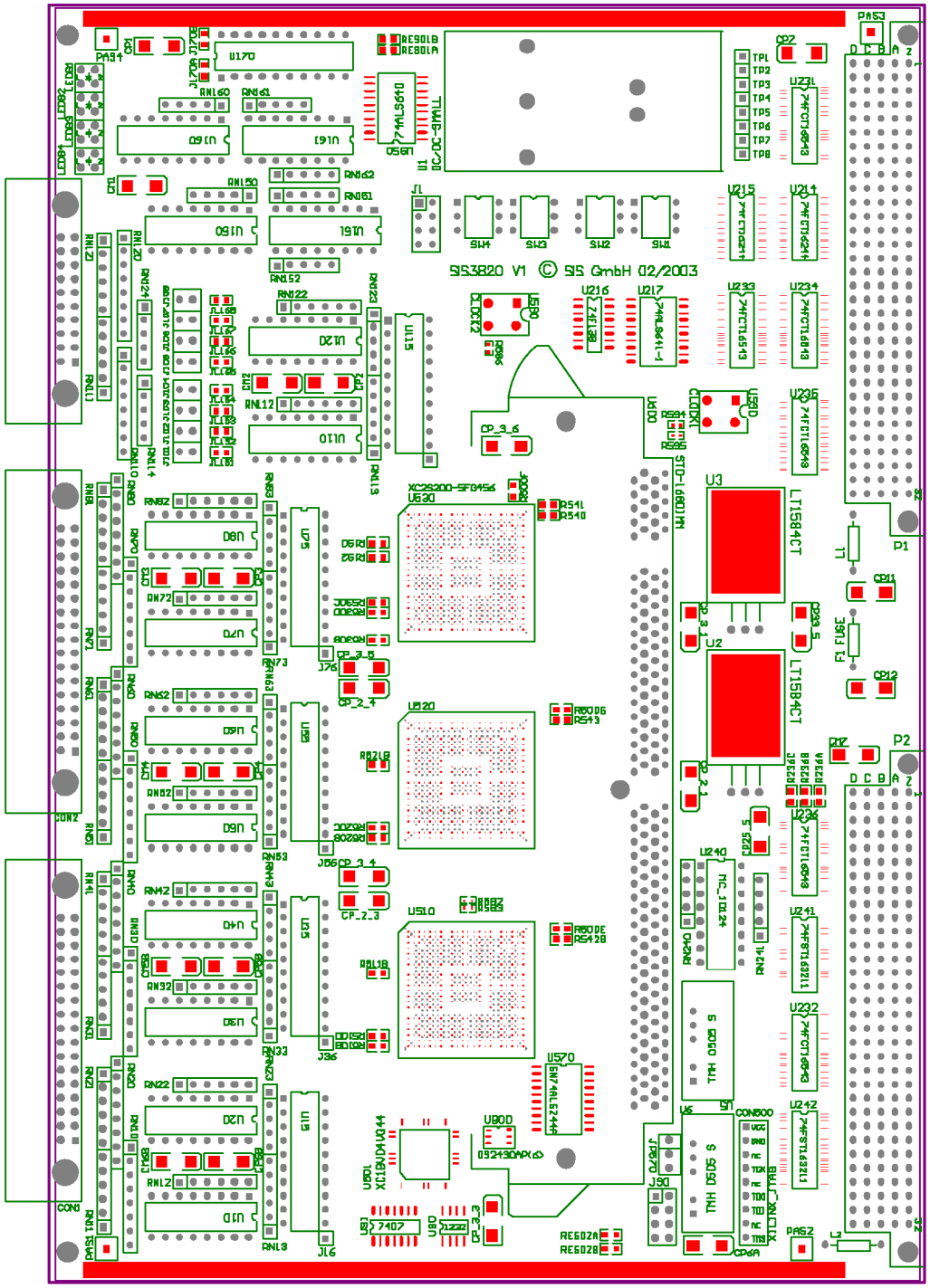
### 8.4.2 16 clock and 16 start/stop/gate mode

The selected clock source is fanned out to 16 of the outputs, the other half of the front panel outputs reflects the start/stop/gate control input.

| Output connector | Signal |
|---|---|
| Odd | Clock |
| Even | Start/stop/gate |

# 9 Board Layout

Find below a printout of the top assembly drawing.



# 10 Jumper settings

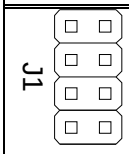
The SIS3820 has 3 jumper fields.

| Jumper field | Function |
|---|---|
| J1 | VME addressing mode |
| J90 | Reset behavior |
| JP570 | JTAG source |
| CON500 | JTAG connector |

The first pin of the jumper fields is marked by a square pin on the solder side and an extra frame on the silk screen of the component side.

## *10.1 J1*

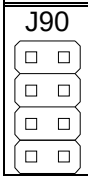
J1 is in charge of the VME addressing mode. The user can select between rotary switch selected A32, A24 and A16 addressing and geographical A32 addressing.. . . A closed position selects the corresponding function.

| | Function |
|---|---|
|   | EN_A32 |
| | EN_A24 |
| | EN_GEO |
| | EN_A16 |

The default setting is EN_A32 closed and all other positions opened.

## *10.2 J90*

J90 controls the reset behavior of the SIS3820.

| | Function |
|---|---|
|   | reserved |
| | connect VME reset to SIS3820 reset |
| | reserved |
| | enable watchdog |

The default setting is VME reset and enable watchdog closed and all other positions opened.

**Note:** open the enable watchdog for firmware upgrades

### *10.3 JP570 JTAG source*

Firmware can be loaded to the XC18V04 serial PROM via a JTAG download cable (XILINX JTAG-PC4 e.g.) or via the VME interface (future option) of the SIS3830. Please note, that errors during this process can render a module temporarily in non working condition.. JP570 has 3 pins. Depending on whether pins 1 and 2 or 2 and 3 are closed the JTAG source is defined as listed below.

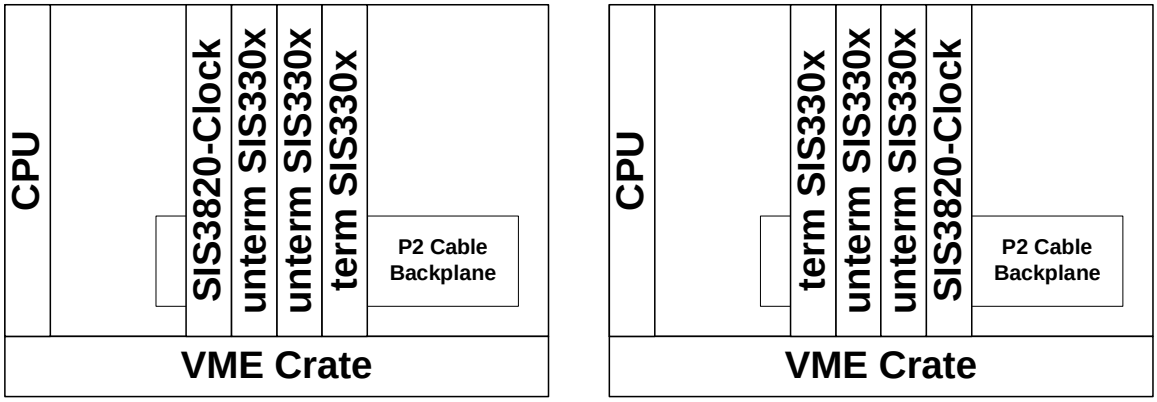
| Closed | JTAG source |
|---|---|
| 1-2 | JTAG connector CON 500 |
| 2-3 | VME |

The default setting is 2-3 closed, i.e. firmware upgrade through JTAG connector

**Note:** VME firmware upgrade capability is not part of the initial SIS3820-CLOCK firmware design.

### *10.4 P2 termination RN240, RN241*

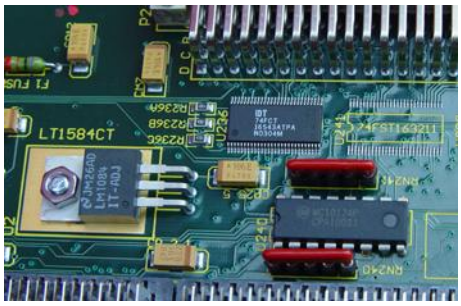
The SIS3820-CLOCK can be used to distribute clock and stop signals to several SIS330x digitizers over a P2 add on (PCB or cable) backplane. The first and the last module on the backplane have to be terminated. The SIS3820-CLOCK can be the first or last module in the chain as illustrated below.




Explanation of shorthands

| Shorthand | Explanation |
|---|---|
| term SIS330x | SIS330x digitizer with termination installed |
| unterm SIS330x | SIS330x digitizer with termination removed |

Termination is installed by default on the SIS3820 as illustrated below.




Default resistor network specification:

| Network | Type | Value |
|---|---|---|
| RN240 | SIL5-1 (5 pins, 4 resistors) | 390 Ω |
| RN241 | SIL5-1 (5 pins, 4 resistors) | 390 Ω |

# 11 Theory of operation

# 12 Appendix

## *12.1 P2 row A/C pin assignments*

The P2 connector of the SIS3820 (in 64 channel or clock module configuration) has connections on rows A and C to feed the second set of 32 inputs to the module or for operation as backplane clock distributor for the SIS330x digitizer family. This implies, that the module can not be operated in a VME slot with a special A/C backplane, like VSB e.g.. The pin assignments of P2 rows A/C of the SIS3820 for both scaler and clock module is shown below. 32 channel versions do not make use of P2 rows A/C.

| P2A | Scaler Function | Clock Function | P2C | Scaler Function | Clock Function |
|---|---|---|---|---|---|
| 1 | not connected | -5.2 V | 1 | not connected | -5.2 V |
| 2 | not connected | -5.2 V | 2 | not connected | -5.2 V |
| 3 | not connected | -5.2 V | 3 | not connected | -5.2 V |
| 4 | not connected | not connected | 4 | not connected | not connected |
| 5 | not connected | not connected | 5 | not connected | not connected |
| 6 | DGND | DGND | 6 | DGND | DGND |
| 7 | Control 1 | P2_CLOCK_H | 7 | Control 0 | P2_CLOCK_L |
| 8 | DGND | DGND | 8 | DGND | DGND |
| 9 | Control 3 | P2_START_H | 9 | Control 2 | P2_START_L |
| 10 | Control 5 | P2_STOP_H | 10 | Control 4 | P2_STOP_L |
| 11 | Control 7 | P2_TEST_H | 11 | Control 6 | P2_TEST_L |
| 12 | DGND | DGND | 12 | DGND | DGND |
| 13 | DGND | DGND | 13 | DGND | DGND |
| 14 | G34_L16 | not connected | 14 | G34_L15 | not connected |
| 15 | G34_L14 | not connected | 15 | G34_L13 | not connected |
| 16 | G34_L12 | not connected | 16 | G34_L12 | not connected |
| 17 | G34_L10 | not connected | 17 | G34_L9 | not connected |
| 18 | G34_L8 | not connected | 18 | G34_L7 | not connected |
| 19 | G34_L6 | not connected | 19 | G34_L5 | not connected |
| 20 | G34_L4 | not connected | 20 | G34_L3 | not connected |
| 21 | G34_L2 | not connected | 21 | G34_L1 | not connected |
| 22 | DGND | DGND | 22 | DGND | DGND |
| 23 | G12_L16 | not connected | 23 | G12_L15 | not connected |
| 24 | G12_L14 | not connected | 24 | G12_L13 | not connected |
| 25 | G12_L12 | not connected | 25 | G12_L11 | not connected |
| 26 | G12_L10 | not connected | 26 | G12_L9 | not connected |
| 27 | G12_L8 | not connected | 27 | G12_L7 | not connected |
| 28 | G12_L6 | not connected | 28 | G12_L5 | not connected |
| 29 | G12_L4 | not connected | 29 | G12_L3 | not connected |
| 30 | G12_L2 | not connected | 30 | G12_L1 | not connected |
| 31 | DGND | DGND | 31 | DGND | DGND |
| 32 | not connected | not connected | 32 | not connected | not connected |

Note: The jumpers for the P2 A/C connections are not soldered in by default on the SIS3820-CLOCK to avoid potential damage by the –5.2 V in conjunction with VSB or similar hardware and to limit –5.2 V power consumption.

### 12.2 Row d and z Pin Assignments

The SIS3820 is ready for the use with VME64x and VME64xP backplanes. Features include geographical addressing (PCB revisions V2 and higher) and live insertion (hot swap). The used pins on the d and z rows of the P1 and P2 connectors are listed below.

| Position | P1/J1 | | P2/J2 | |
|---|---|---|---|---|
| | Row z | Row d | Row z | Row d |
| 1 | | VPC (1) | | |
| 2 | GND | GND (1) | GND | |
| 3 | | | | |
| 4 | GND | | GND | |
| 5 | | | | |
| 6 | GND | | GND | |
| 7 | | | | |
| 8 | GND | | GND | |
| 9 | | GAP* | | |
| 10 | GND | GA0* | GND | |
| 11 | RESP* | GA1* | | |
| 12 | GND | | GND | |
| 13 | | GA2* | | |
| 14 | GND | | GND | |
| 15 | | GA3* | | |
| 16 | GND | | GND | |
| 17 | | GA4* | | |
| 18 | GND | | GND | |
| 19 | | | | |
| 20 | GND | | GND | |
| 21 | | | | |
| 22 | GND | | GND | |
| 23 | | | | |
| 24 | GND | | GND | |
| 25 | | | | |
| 26 | GND | | GND | |
| 27 | | | | |
| 28 | GND | | GND | |
| 29 | | | | |
| 30 | GND | | GND | |
| 31 | | GND (1) | | GND (1) |
| 32 | GND | VPC (1) | GND | VPC (1) |

**Note: Pins designated with (1) are so called MFBL (mate first-break last) pins on the installed 160 pin connectors, VPC(1) pins are connected via inductors.**

## 12.3 Connector Types

Find below a list of connector types that are used on the SIS3820.

| Connector | Purpose | Part Number |
|---|---|---|
| 160 pin zabcd | VME P1/P2 | Harting 02 01 160 2101 |
| 20 pin header | Control (flat cable versions) | DIN41651 20 Pin (AMP e.g.) |
| 34 pin header | Inputs (flat cable versions) | DIN41651 34 Pin (AMP e.g.) |
| LEMO | Control and Input (LEMO versions) | LEMO ERN.00.250.CTL |
| SDRAM | SDRAM memory socket | Berg 88638-60002 |

## 12.4 Power consumption

The SIS3820 is a single +5 V supply board. Lower positive voltages (3.3 V and 2.5 V) are generated with low dropout regulators. –5 V is generated with up to 3 DC/DC converters.

| Board type | Voltage | Current |
|---|---|---|
| SIS3820-SCALER (32 ECL channels) | 5 V | 2.0 A |
| SIS3820-SCALER (32 TTL channels) | 5 V | 1.3A |
| SIS3820-CLOCK | 5 V | 3.2 A |

## 12.5 Operating conditions

### 12.5.1 Cooling

Hence Forced air flow is required for the operation of the SIS3820 board. The board may be operated in a non condensing environment at an ambient temperature between 10° and 40° Celsius.

### 12.5.2 Hot swap/live insertion

Please note, that the VME standard does not support hot swap by default. The SIS3820 is configured for hot swap in conjunction with a VME64x backplane. In non VME64x backplane environments the crate has to be powered down for module insertion and removal.

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